

## Revision:2.31

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[illegible]

<b>GIGABYTE</b>			
Title			
<b>BLOCK DIAGRAM</b>			
Size	Document Number		Rev
Custom	<b>GA-M52LT-D3</b>		<b>2.3</b>
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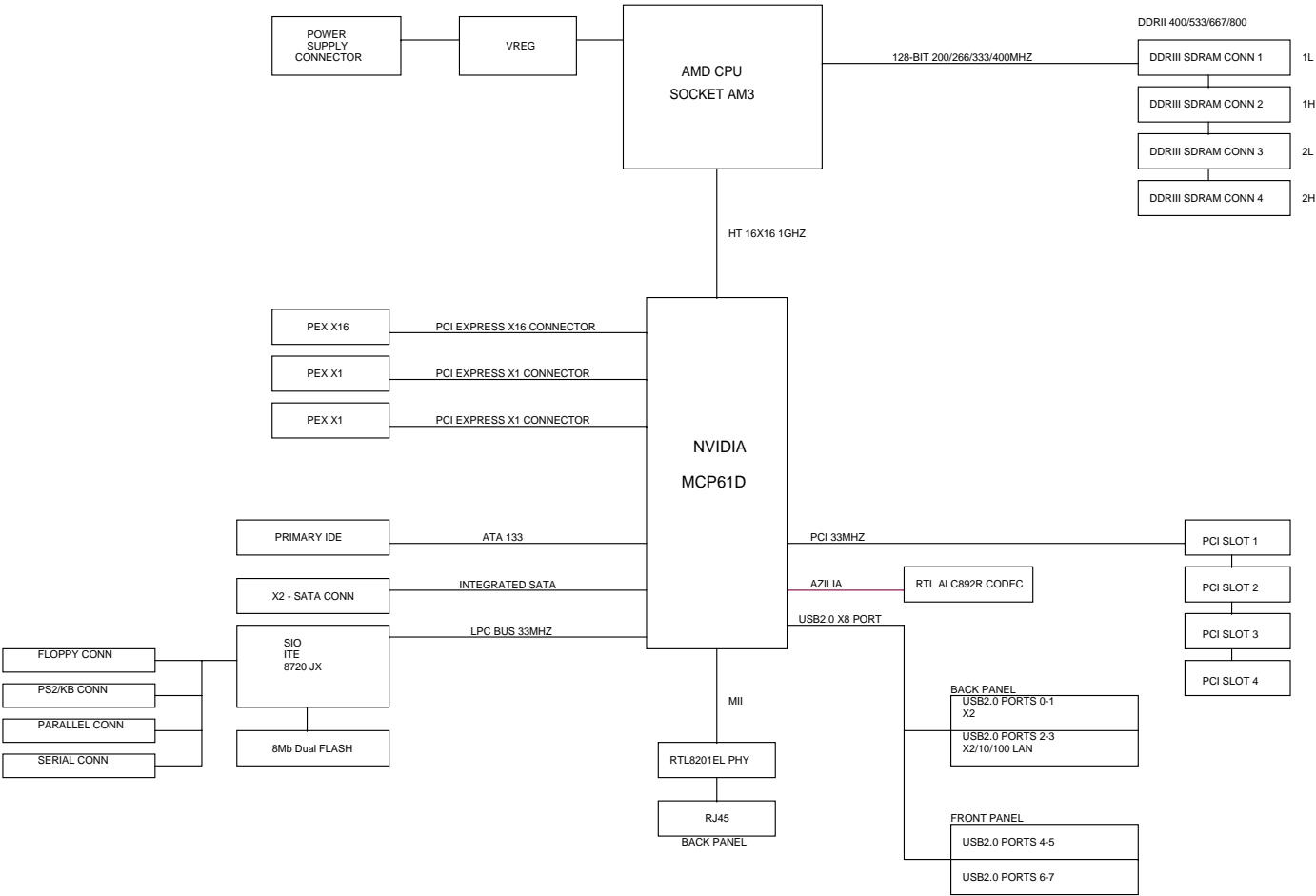
**P-Code: U96058-0**

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

[illegible]

<b>GIGABYTE</b>			
<b>Title</b> <b>BOM &amp; PCB MODIFY HISTORY</b>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	
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BLOCK DIAGRAM



<u>L0_CADIN_L[0..15]</u>	<L0_CADIN_L[0..15]	<10>
<u>L0_CADIN_H[0..15]</u>	<L0_CADIN_H[0..15]	<10>
<u>L0_CLKIN_L[0..1]</u>	<L0_CLKIN_L[0..1]	<10>
<u>L0_CLKIN_H[0..1]</u>	<L0_CLKIN_H[0..1]	<10>
<u>L0_CADOUT_L[0..15]</u>	<L0_CADOUT_L[0..15]	<10>
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**MCP602A**

**HYPERTRANS**

VCC12\_HT

R3

R4

49.9/41

49.9/41

<10> L0\_CTIN\_L0

<10> L0\_CTIN\_L0

L0\_CLKIN\_H1 N6

L0\_CLKIN\_L1 P6

L0\_CLKIN\_H0 N3

L0\_CLKIN\_N2 N2

L0\_CLKIN\_H(15)

L0\_CADIN\_L15 U6

L0\_CADIN\_H14 T4

L0\_CADIN\_L14 T5

L0\_CADIN\_H13 R6

L0\_CADIN\_L13 T6

L0\_CADIN\_H12 P4

L0\_CADIN\_L12 P5

L0\_CADIN\_H11 M4

L0\_CADIN\_L11 M5

L0\_CADIN\_H10 L6

L0\_CADIN\_L10 M6

L0\_CADIN\_H9 K4

L0\_CADIN\_L9 J5

L0\_CADIN\_H8 J6

L0\_CADIN\_L8 K6

L0\_CADIN\_H7 U3

L0\_CADIN\_L7 U2

L0\_CADIN\_H6 R1

L0\_CADIN\_L6 L6

L0\_CADIN\_H5 R3

L0\_CADIN\_L5 R2

L0\_CADIN\_H4 N1

L0\_CADIN\_L4 P1

L0\_CADIN\_H3 L1

L0\_CADIN\_L3 M1

L0\_CADIN\_H2 L3

L0\_CADIN\_L2 L2

L0\_CADIN\_H1 K1

L0\_CADIN\_L1 J1

L0\_CADIN\_H0 J3

L0\_CADIN\_L0 J2

L0\_CLKOUT\_H(1) A05

L0\_CLKOUT\_L(1) A04

L0\_CLKOUT\_H(0) A01

L0\_CLKOUT\_L(0) AC1

L0\_CADOUT\_H(15) Y5

L0\_CADOUT\_L(15) Y4

L0\_CADOUT\_H(14) AB6

L0\_CADOUT\_L(14) AA6

L0\_CADOUT\_H(13) AB5

L0\_CADOUT\_L(13) AB4

L0\_CADOUT\_H(12) AD6

L0\_CADOUT\_L(12) AC6

L0\_CADOUT\_H(11) AF6

L0\_CADOUT\_L(11) AF5

L0\_CADOUT\_H(10) AF4

L0\_CADOUT\_L(10) AH6

L0\_CADOUT\_H(9) AG6

L0\_CADOUT\_L(9) AH5

L0\_CADOUT\_H(8) AH4

L0\_CADOUT\_L(8) Y1

L0\_CADOUT\_H(7) W1

L0\_CADOUT\_L(7) AA2

L0\_CADOUT\_H(6) AA3

L0\_CADOUT\_L(6) AB1

L0\_CADOUT\_H(5) AA1

L0\_CADOUT\_L(5) AC2

L0\_CADOUT\_H(4) AC3

L0\_CADOUT\_L(4) AE2

L0\_CADOUT\_H(3) AE3

L0\_CADOUT\_L(3) AF1

L0\_CADOUT\_H(2) AE1

L0\_CADOUT\_L(2) AG2

L0\_CADOUT\_H(1) AG3

L0\_CADOUT\_L(1) AH1

L0\_CADOUT\_H(0) AG1

L0\_CADOUT\_L(0)

TP78

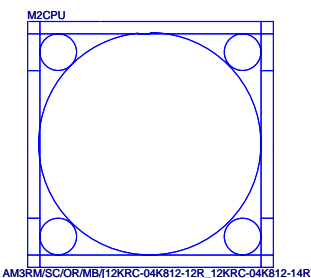
TP79

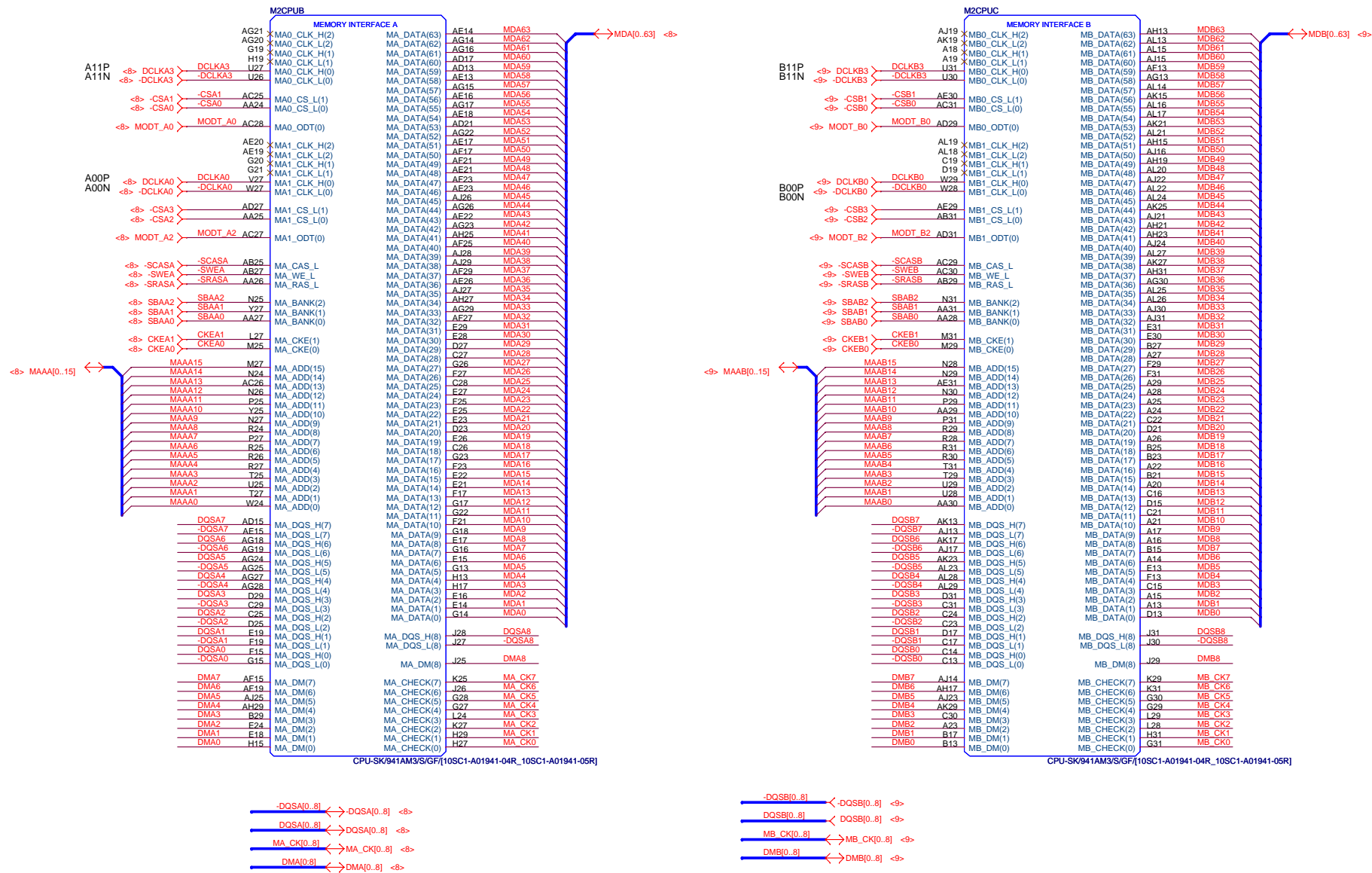
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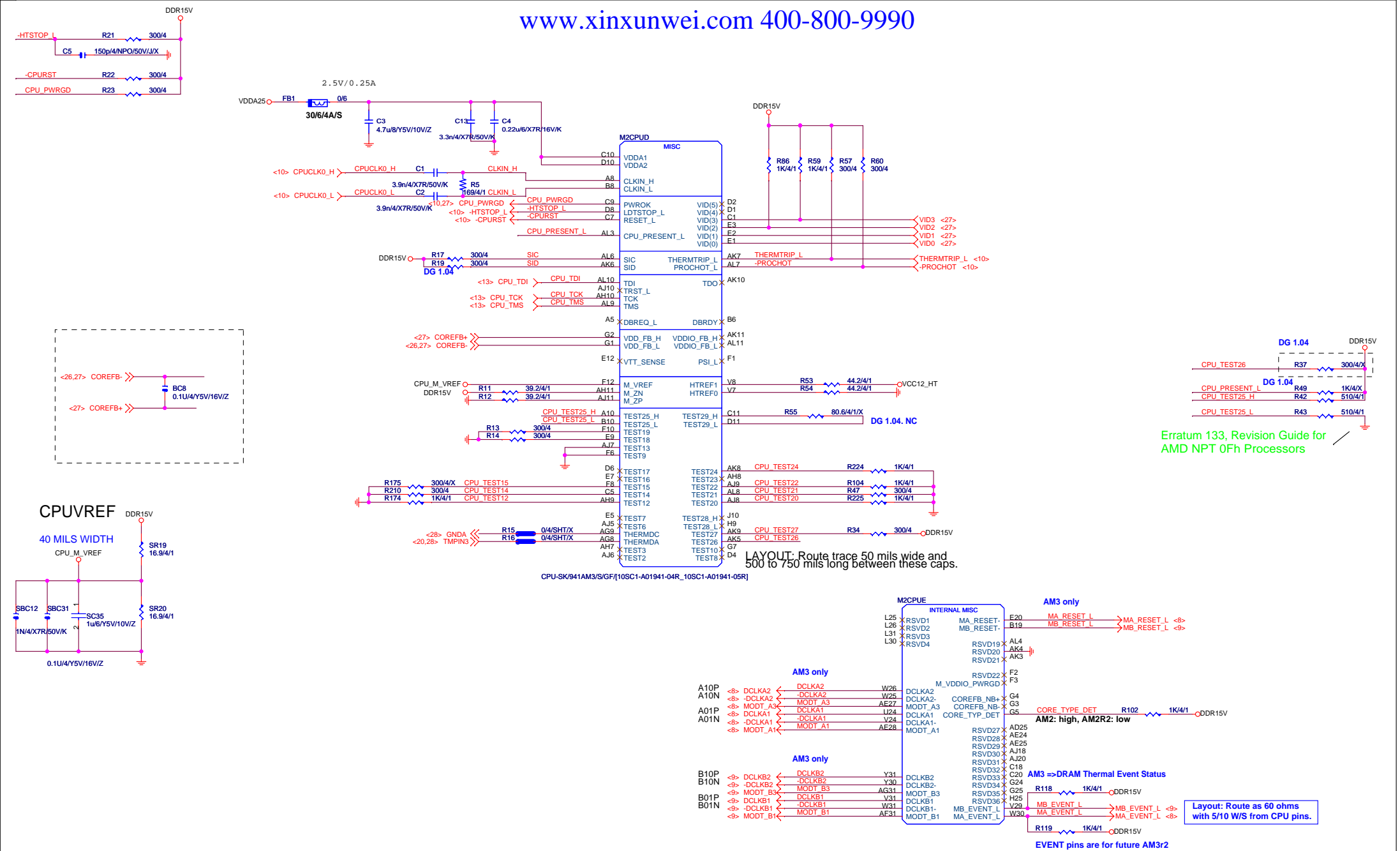
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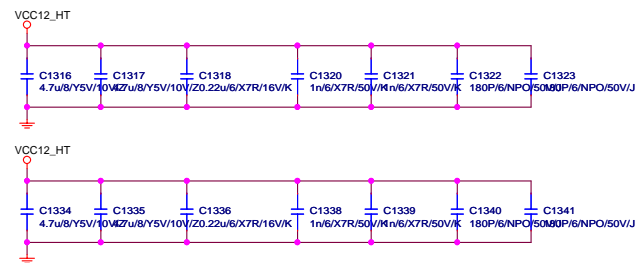
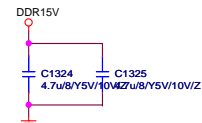
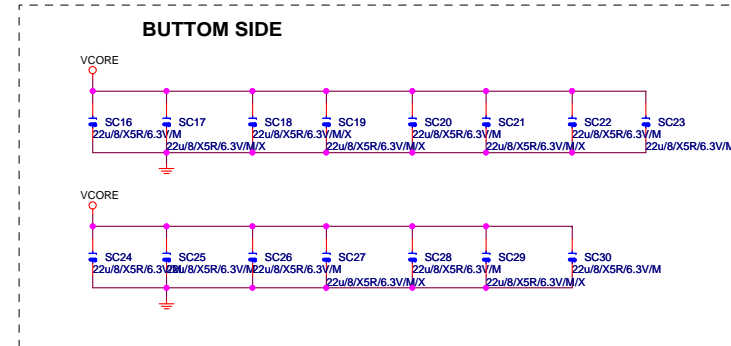
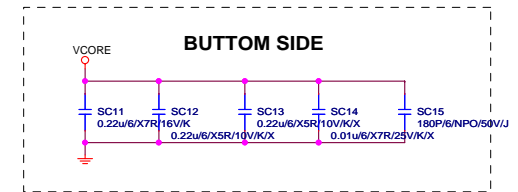
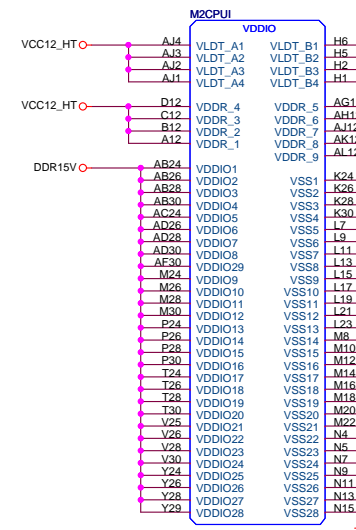
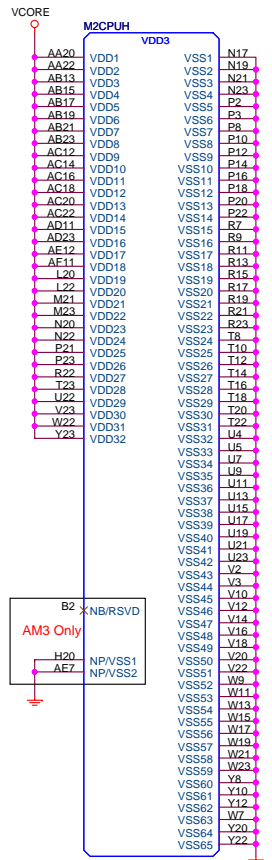
```
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT
```

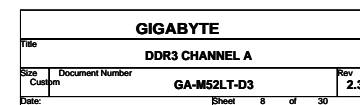
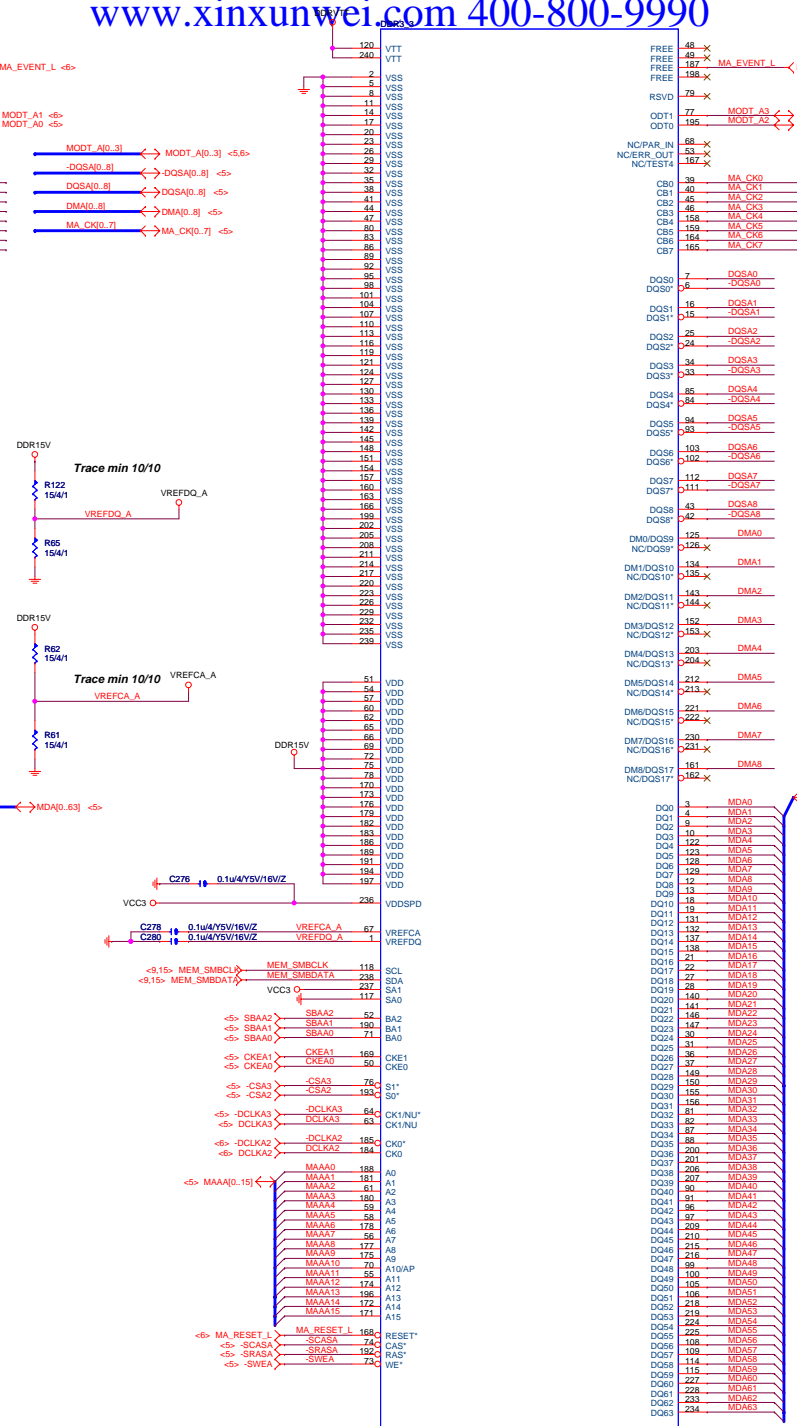
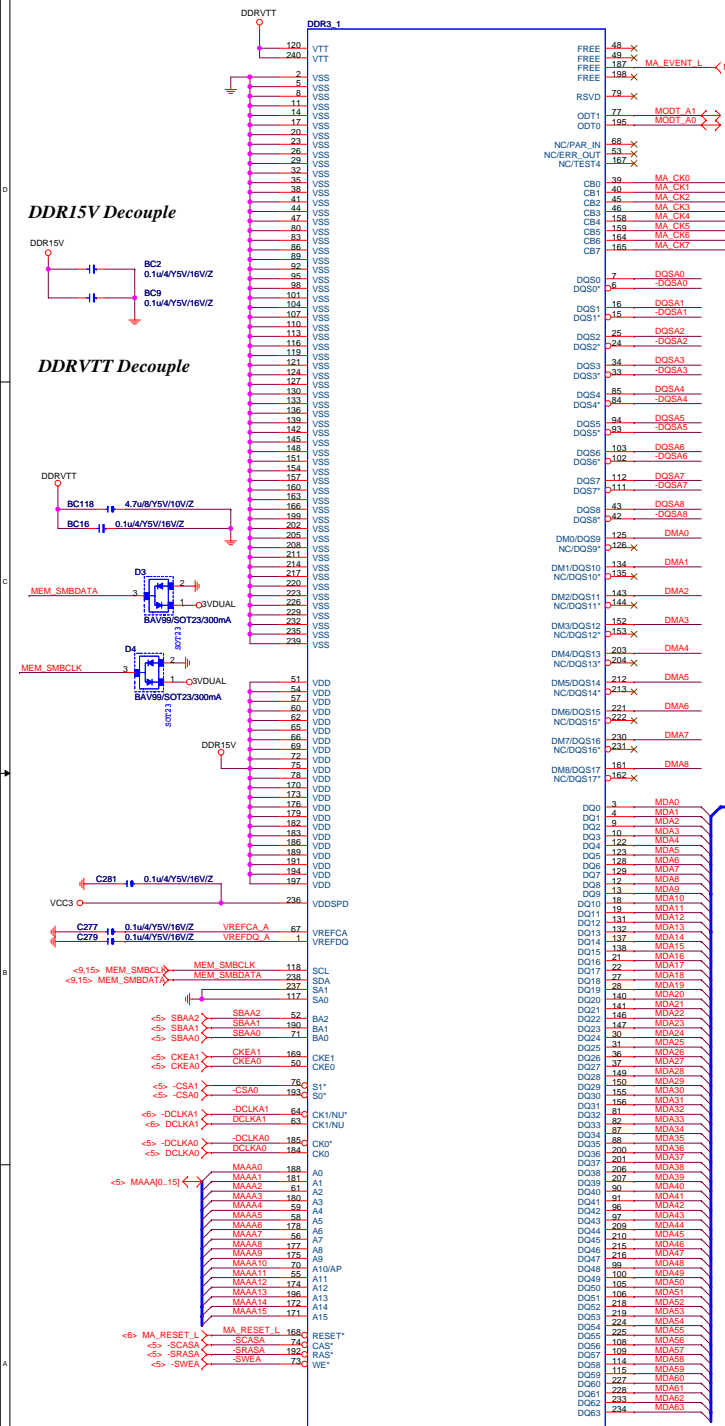
```
VLDT_A = VCC12_HT
VLDT_B = HT12B
```



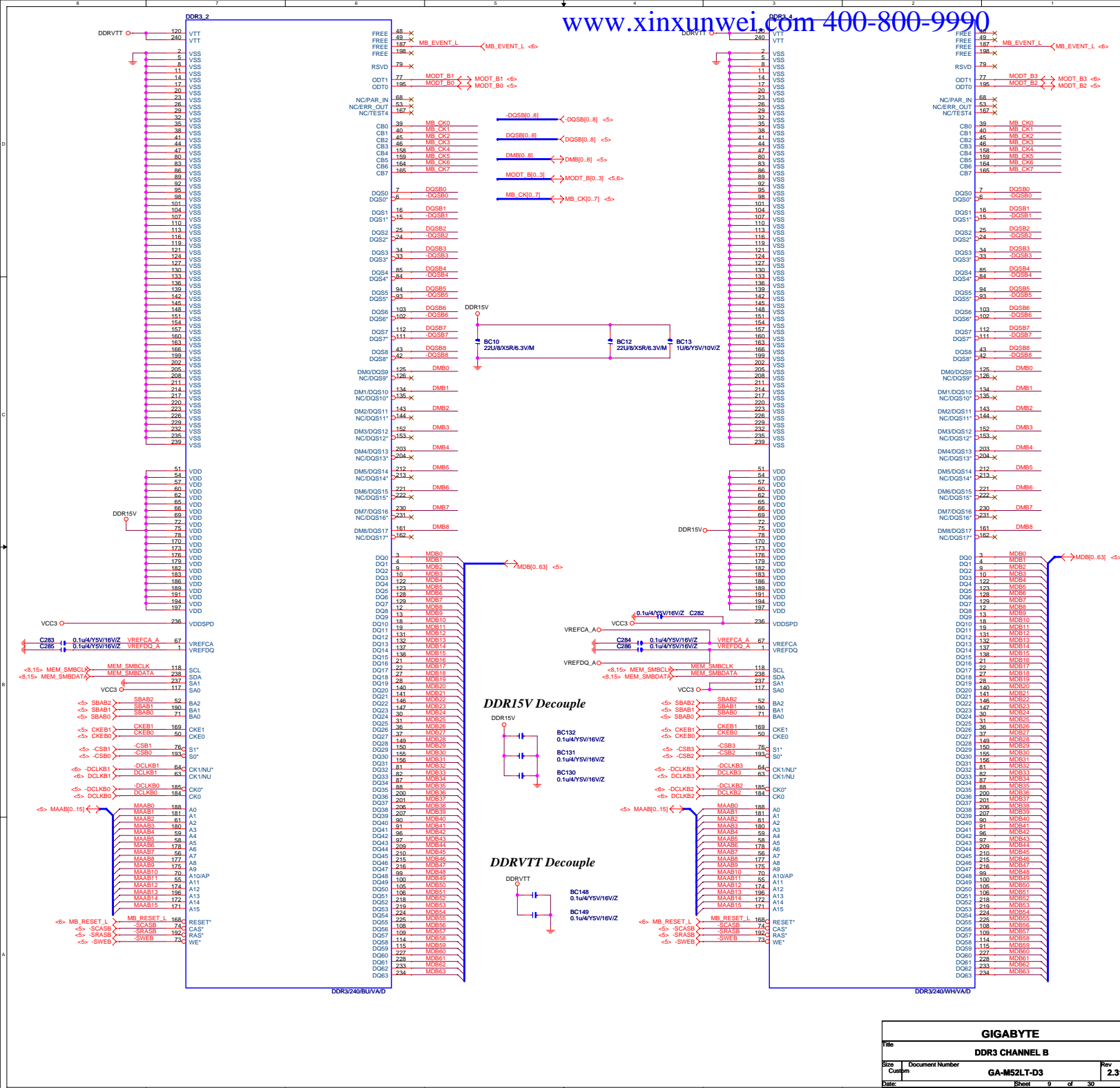


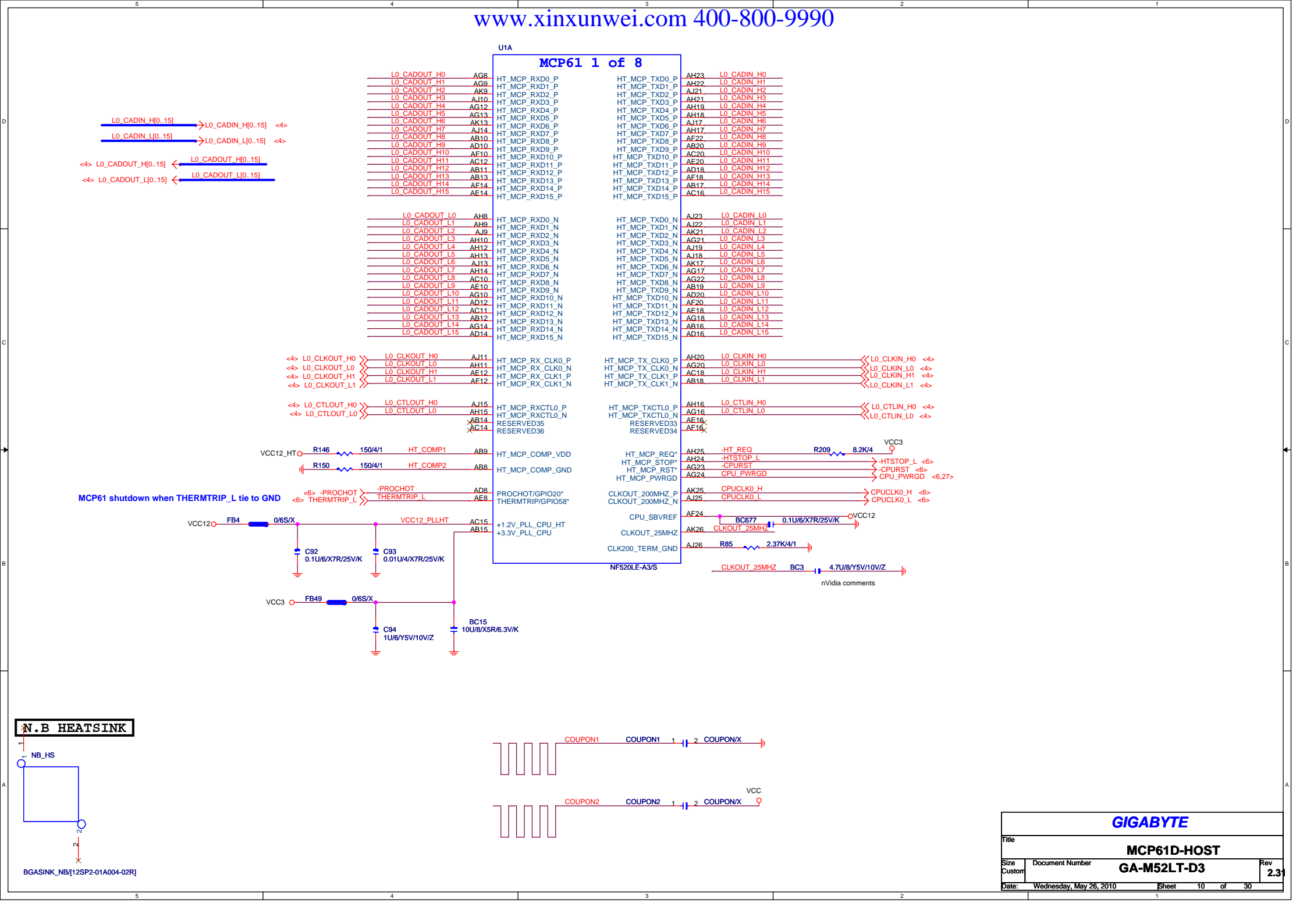
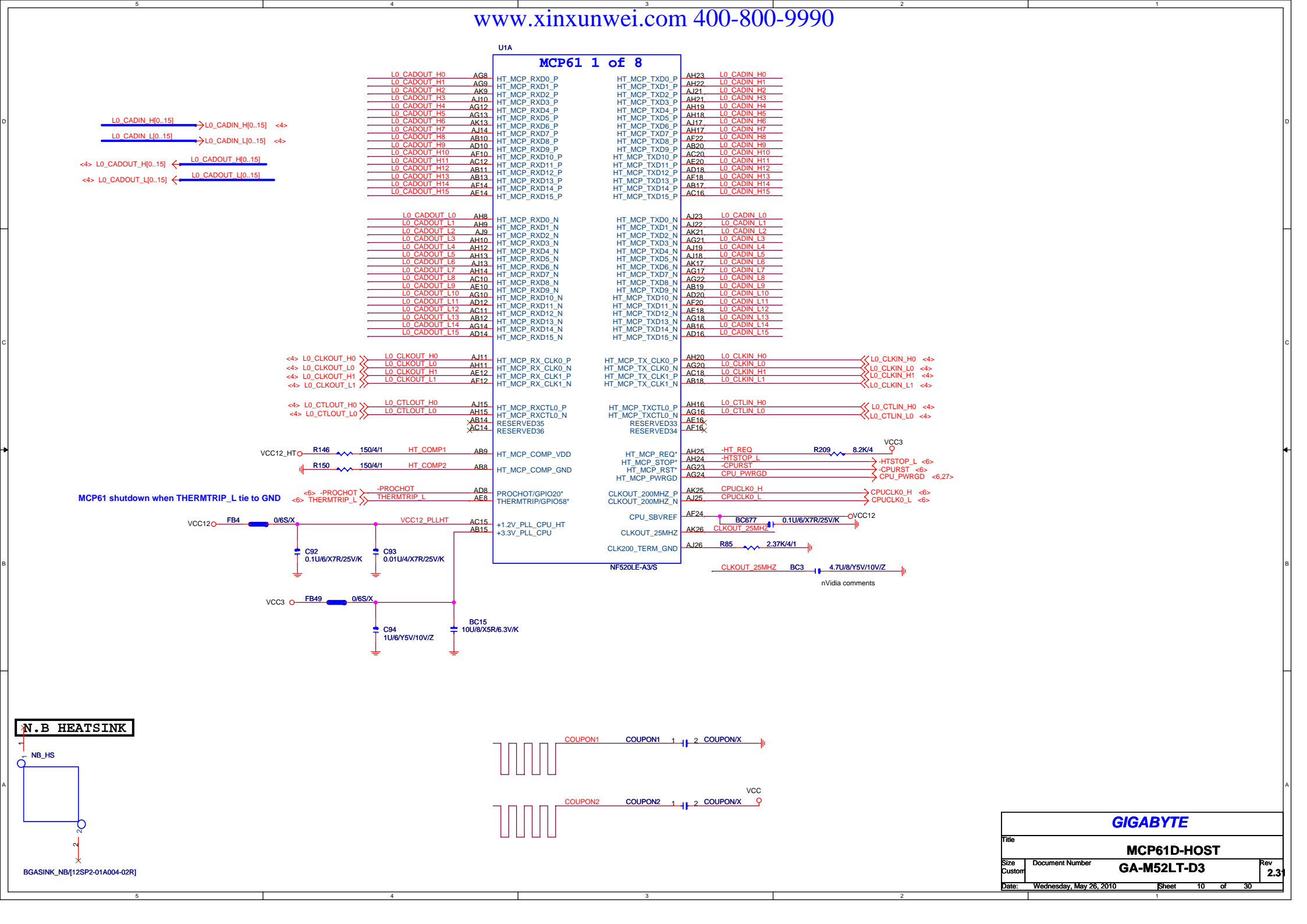
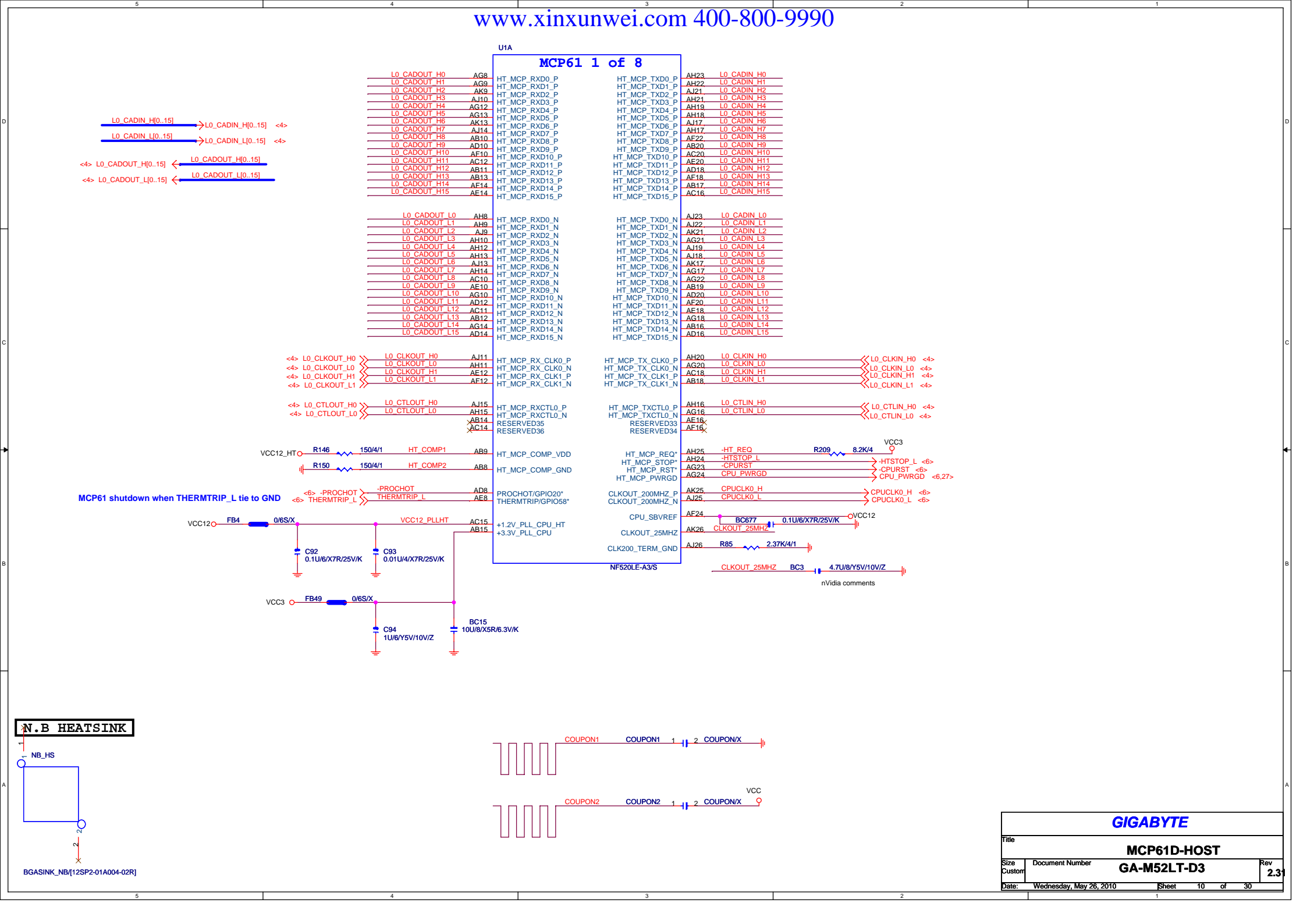


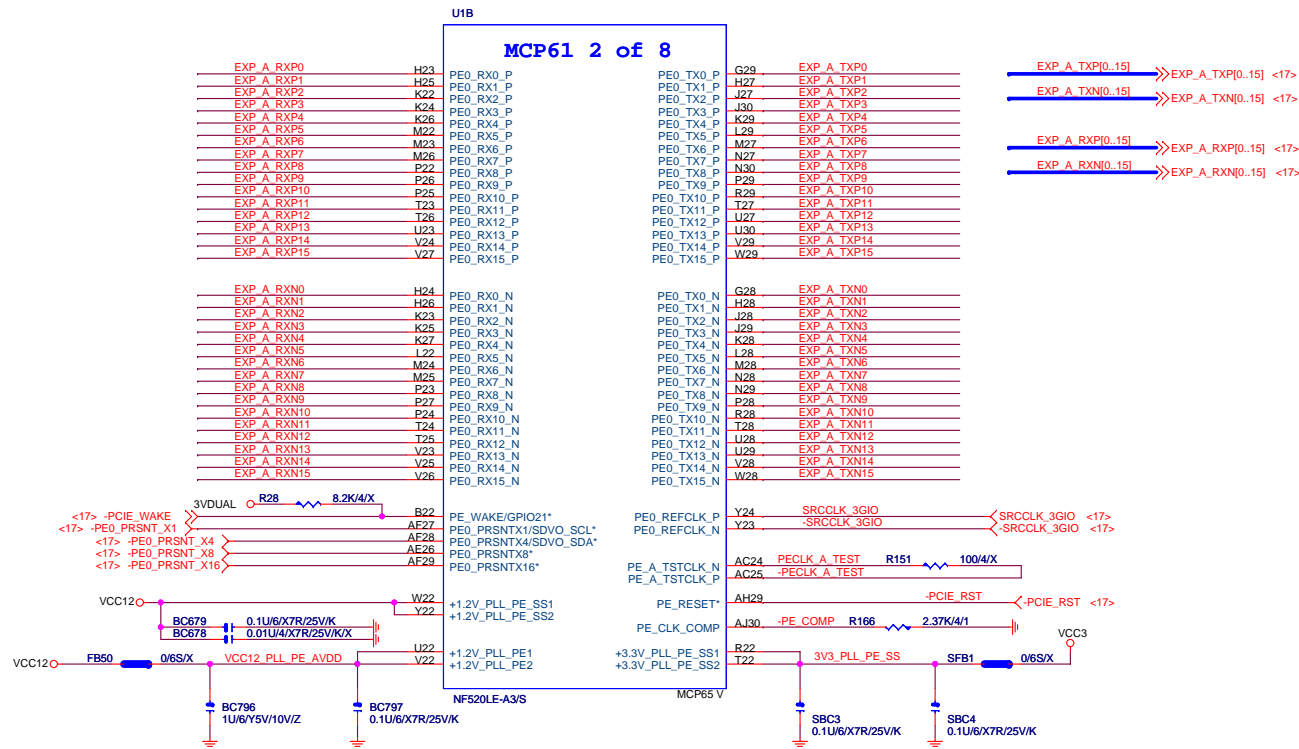








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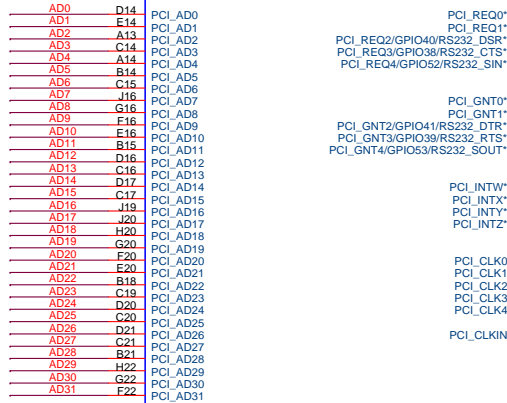
GIGABYTE

Title			MCP61D-PCI_E
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U1D

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PCI\_REQ0\*  
PCI\_REQ1\*  
PCI\_REQ2/GPIO40/RS232\_DS\*  
PCI\_REQ3/GPIO38/RS232\_CTS\*  
PCI\_REQ4/GPIO52/RS232\_SIN\*

PCI\_GNT0\*  
PCI\_GNT1\*  
PCI\_GNT2/GPIO41/RS232\_DTR\*  
PCI\_GNT3/GPIO39/RS232\_RTS\*  
PCI\_GNT4/GPIO53/RS232\_SOUT\*

PCI\_INTW\*  
PCI\_INTX\*  
PCI\_INTY\*  
PCI\_INTZ\*

PCI\_CLK0  
PCI\_CLK1  
PCI\_CLK2  
PCI\_CLK3  
PCI\_CLK4

PCI\_CLKIN

G12 -REQ0 > REQ0 <18>  
A10 -REQ1 > REQ1 <18>  
C11 -REQ2 > REQ2 <18>  
H14 -REQ3 > REQ3 <18>  
D13 -REQ4 > REQ4 <19>

A9 -GNT0 > GNT0 <18>  
C10 -GNT1 > GNT1 <18>  
J14 -GNT3 > GNT3 <18>  
C12 -GNT4 > GNT4 <19>

C22 -INTA > INTA <18,19>  
D22 -INTB > INTB <18,19>  
A22 -INTC > INTC <18,19>  
A21 -INTD > INTD <18,19>

B13 PCLK0 R67 22/4 PCICLK1 > PCICLK1 <18>  
F14 PCLK1 R69 22/4 PCICLK2 > PCICLK2 <18>  
D12 PCLK2 R36 22/4 PCICLK5 > PCICLK5 <19>  
H12 PCLK4 R227 22/4 PCICLK4 > PCICLK4 <18>

J12 -PCICLK\_FB

<15,23> ACZ\_SDOUT <-> ACZ\_SDOUT R41 1K/4/1 nVidia comment  
-LFRAME R40 1K/4/1 nVidia comment

-GNT4 R200 8.2K/4 VCC3  
-REQ4 R81 8.2K/4 VCC3  
-PCIPME R78 8.2K/4 3VDUAL

PCICLK4 C86 10P/4/N/50V/X  
PCICLK5 C89 10P/4/N/50V/X  
LPC33 C84 10P/4/NPO/50V/J  
PCICLK\_FB BC217 10P/4/N/50V/X EMI

<18,19> -C\_BE0 <-> -C\_BE0 H16 PCI\_CBE0\*  
<18,19> -C\_BE1 <-> -C\_BE1 B17 PCI\_CBE1\*  
<18,19> -C\_BE2 <-> -C\_BE2 A18 PCI\_CBE2\*  
<18,19> -C\_BE3 <-> -C\_BE3 B19 PCI\_CBE3\*

<18,19> -FRAME <-> -FRAME C18 PCI\_FRAME\*  
<18,19> -IRDY <-> -IRDY A17 PCI\_IRDY\*  
<18,19> -TRDY <-> -TRDY D18 PCI\_TRDY\*  
<18,19> -STOP <-> -STOP E18 PCI\_STOP\*  
<18,19> -DEVSEL <-> -DEVSEL E18 PCI\_DEVSEL\*  
<18,19> PAR <-> PAR J18 PCI\_PAR\*  
<18,19> -PERR <-> -PERR G18 PCI\_PERR/GPIO43/RS232\_DCD\*  
<18,19> -SERR <-> -SERR H18 PCI\_SERR\*  
<18,19> -PCIPME <-> -PCIPME E22 PCI\_PME/GPIO30\*

LPC\_AD0  
LPC\_AD1  
LPC\_AD2  
LPC\_AD3

PCI\_RESET0\*  
PCI\_RESET1\*  
PCI\_RESET2\*  
PCI\_RESET3\*  
LPC\_RESET\*

LPC\_PWRDN#/GPIO54/EXT\_NMI\*  
LPC\_FRAME\*  
LPC\_DRQ0/GPIO50\*  
LPC\_DRQ1/GPIO15/FAIR/PMI\*  
LPC\_SERIRQ

C8 -NV\_TCK  
H10 -LFRAME <-> -LFRAME <28>  
C9 -LDRQ0 <-> -LDRQ0 <28>  
B9 -LDRQ1 <-> -LDRQ1 <28>  
J10 -SERIRQ <-> -SERIRQ <28>

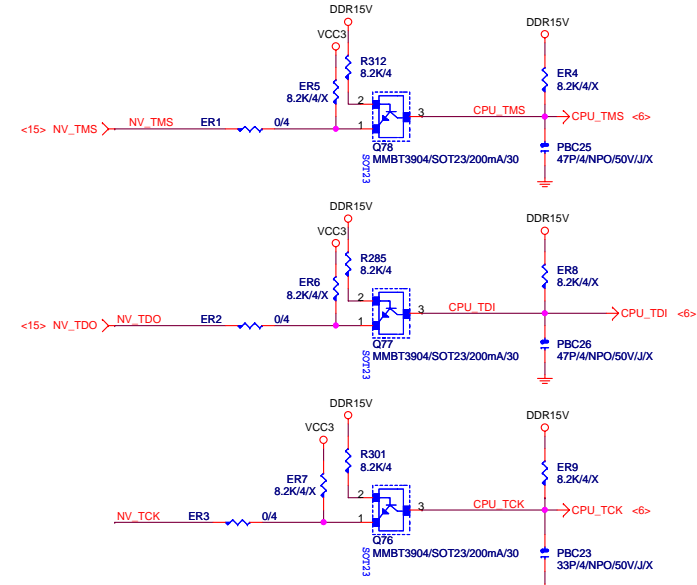
R76 8.2K/4/X VCC3  
nVidia comment

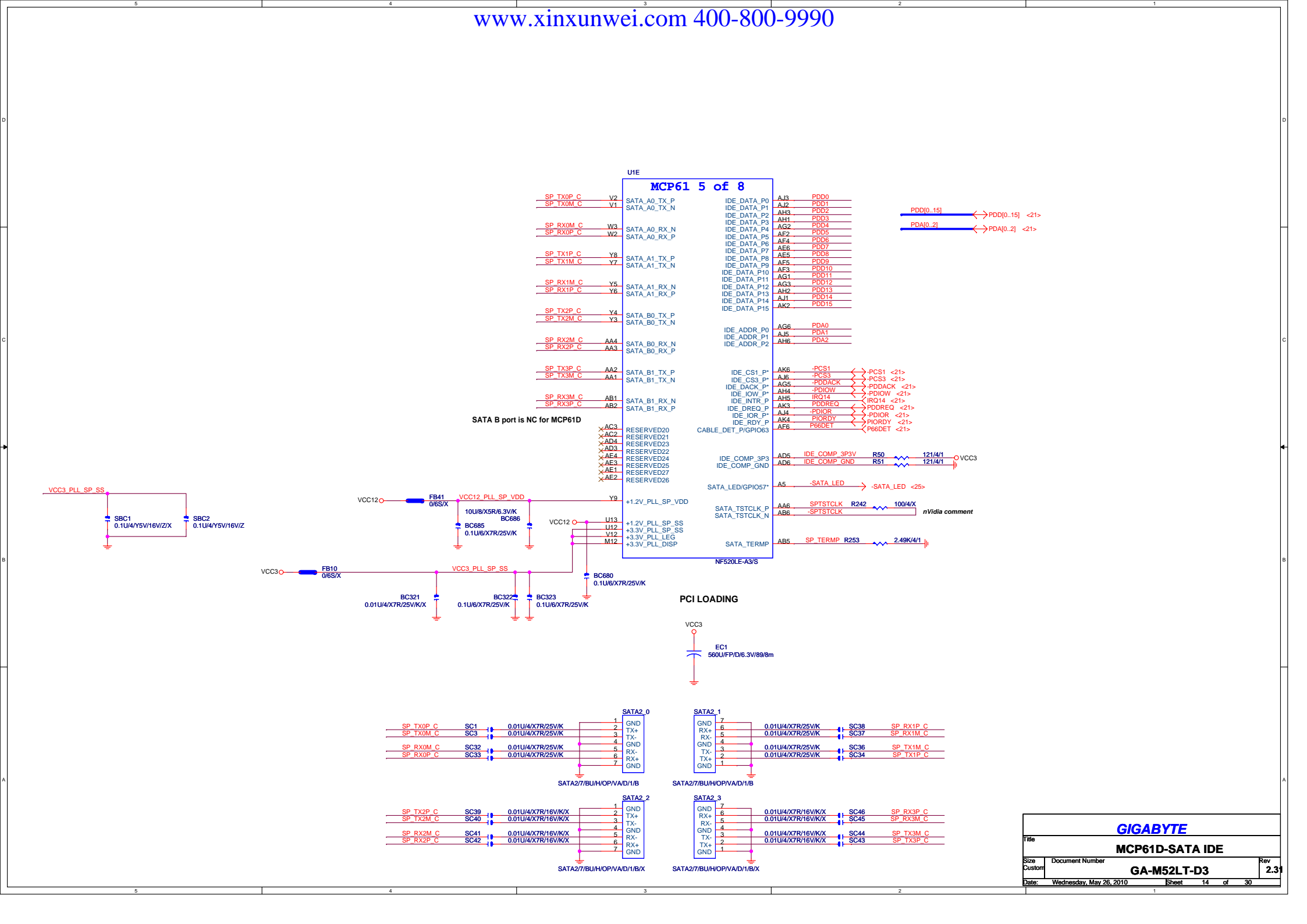
E8 R84 33/4 LPC33 > LPC33 <28>  
D8 X

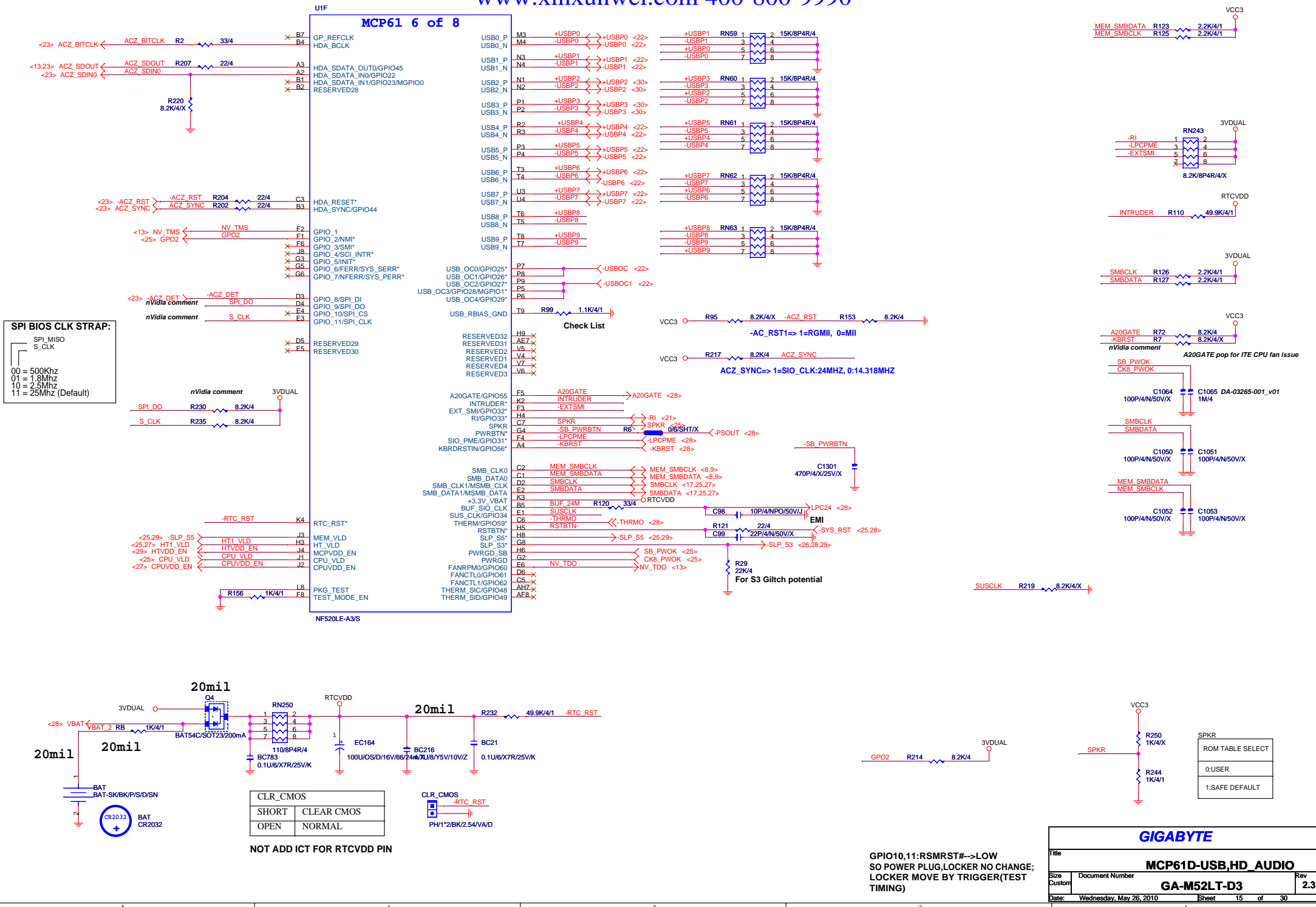
NF520LE-A3/S

BIOS STRAP:

ACZ\_SDOUT  
-LFRAME  
0 0 = LPC BIOS  
0 1 = PCI BIOS  
1 0 = SPI BIOS(Default)  
1 1 = RESERVED

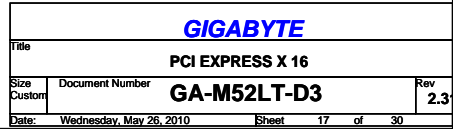


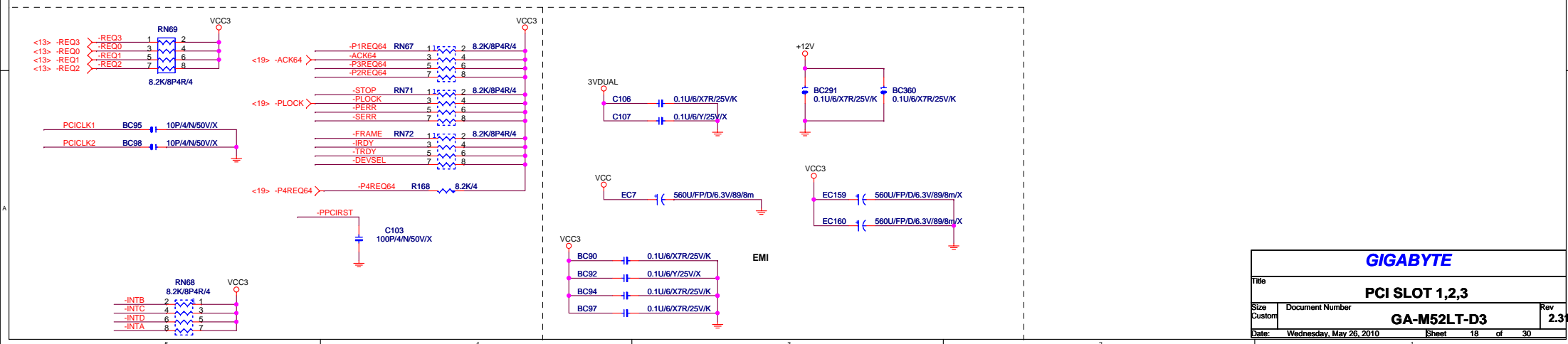
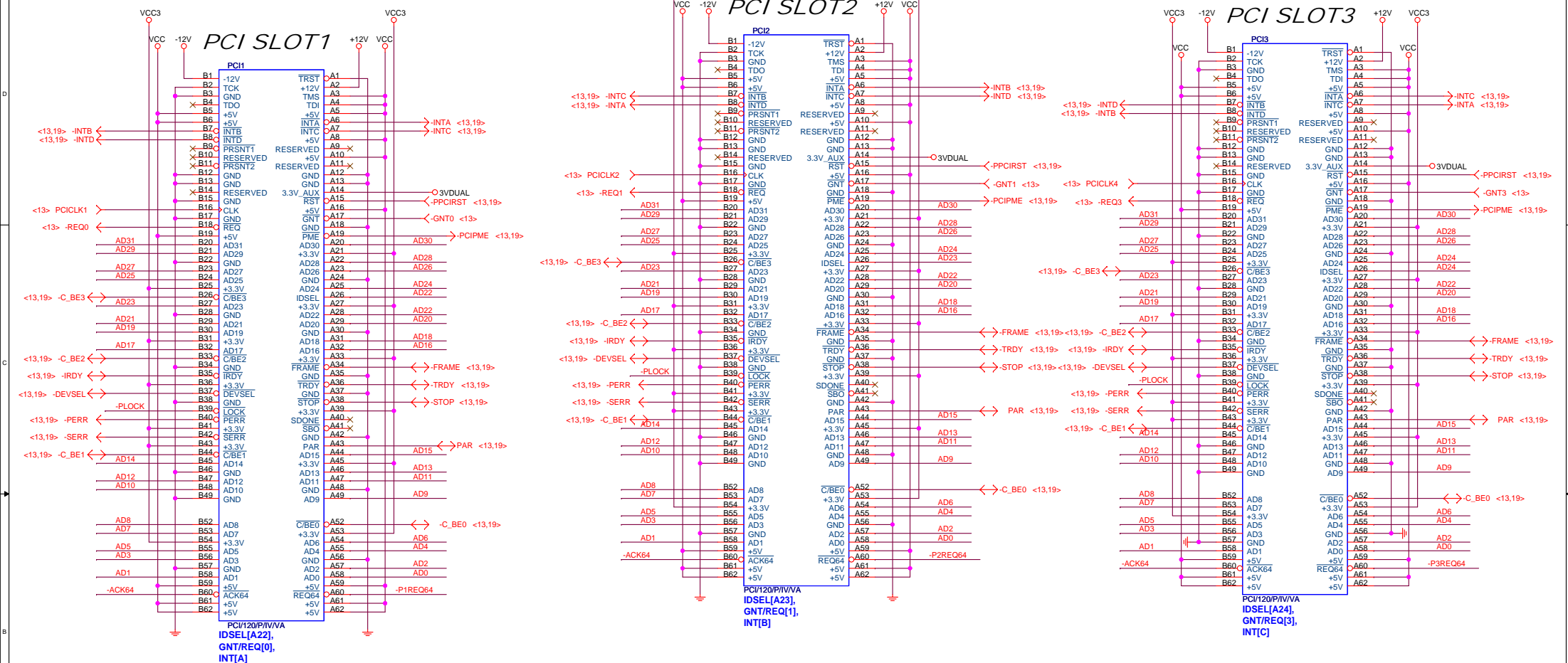


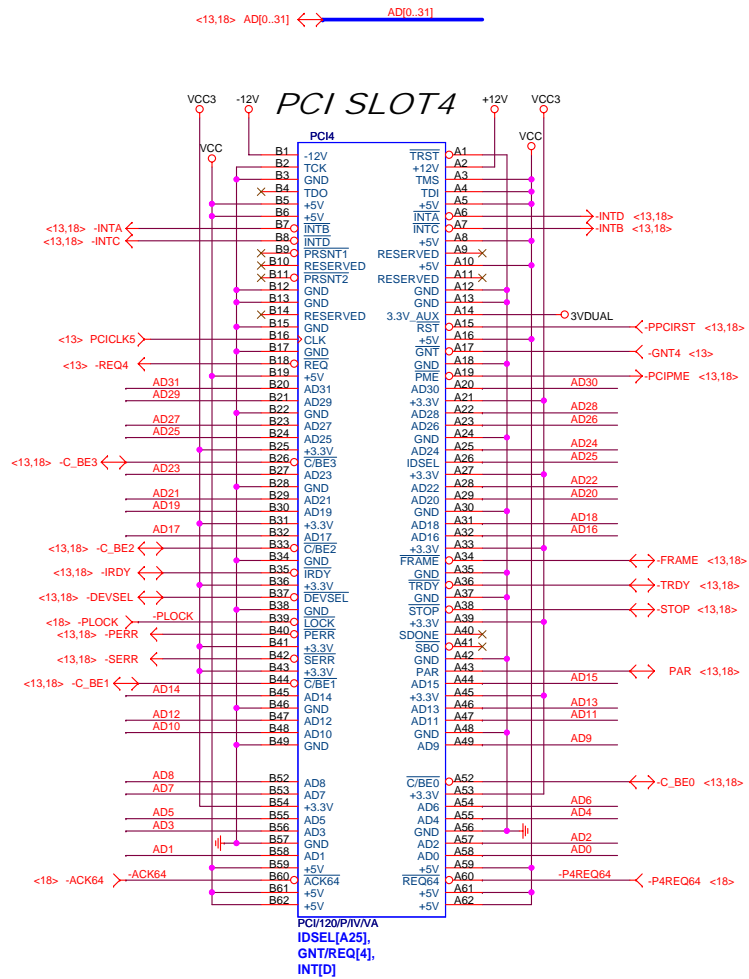






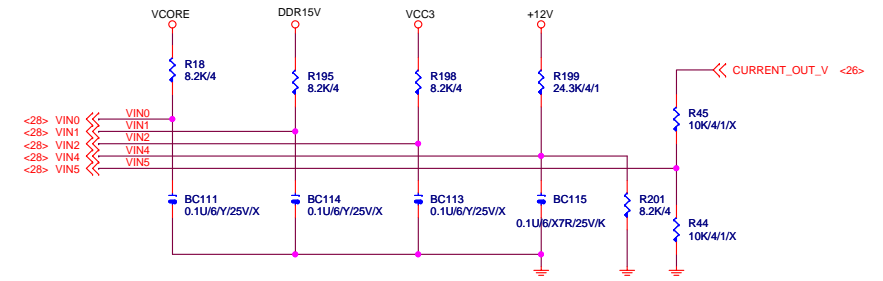
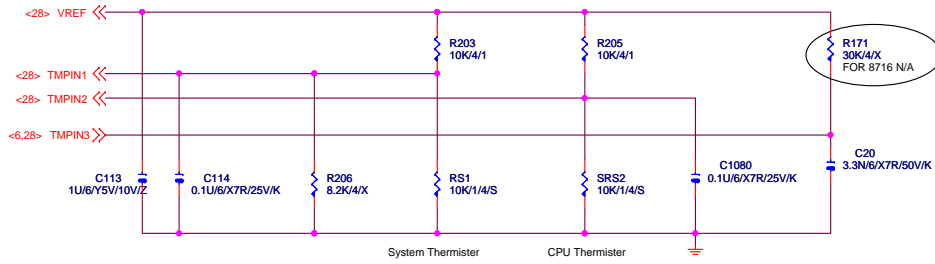




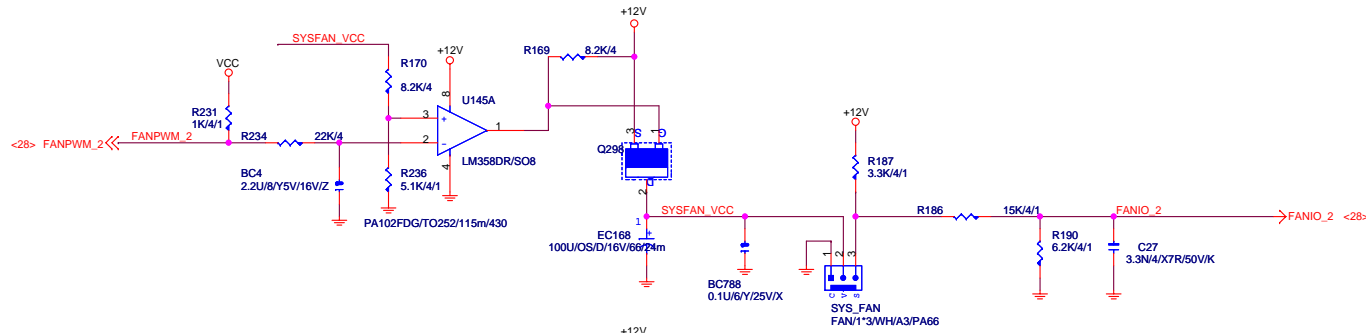


GIGABYTE			
PCI SLOT 4			
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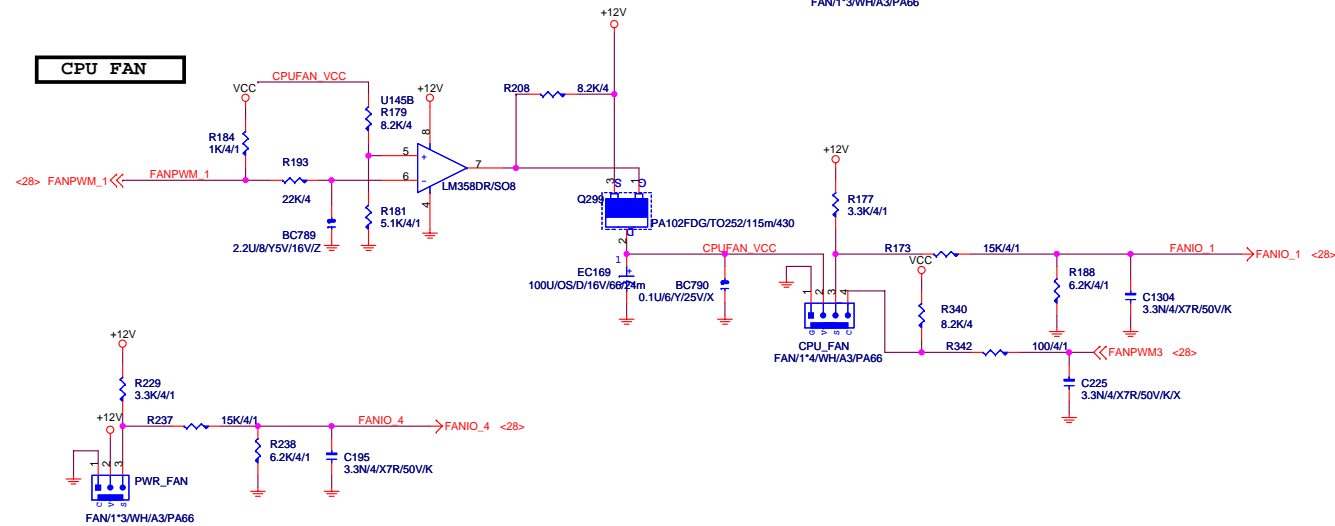
## Hardware Monitor circuits



## SYSTEM FAN



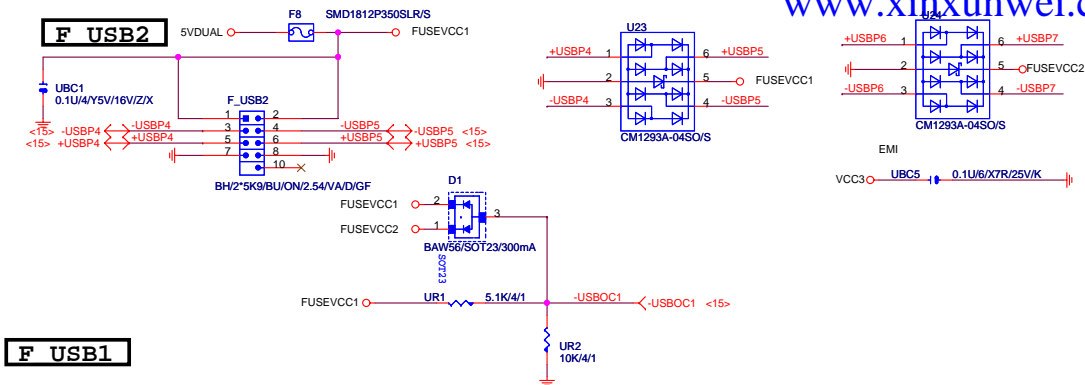
## CPU FAN

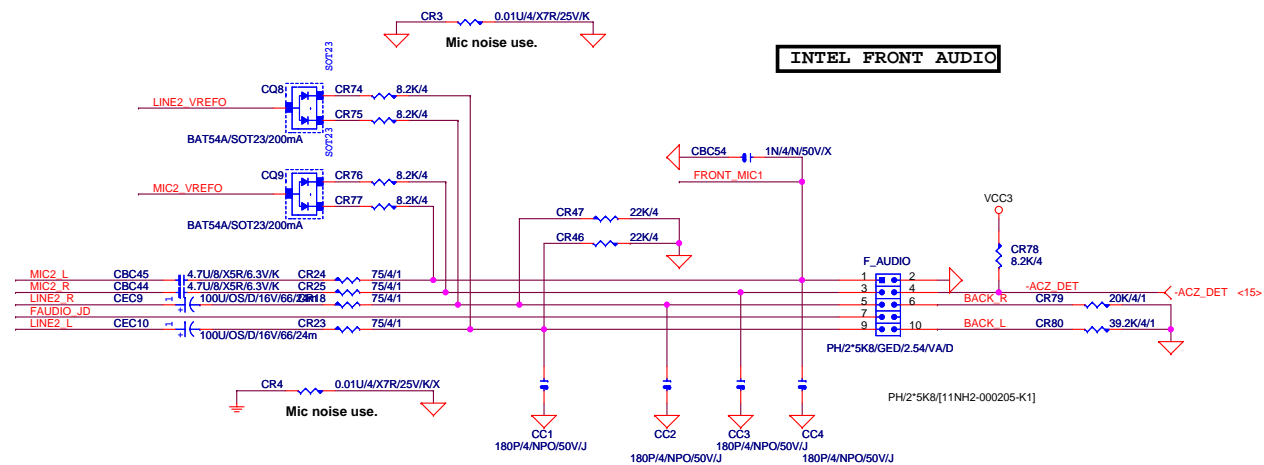
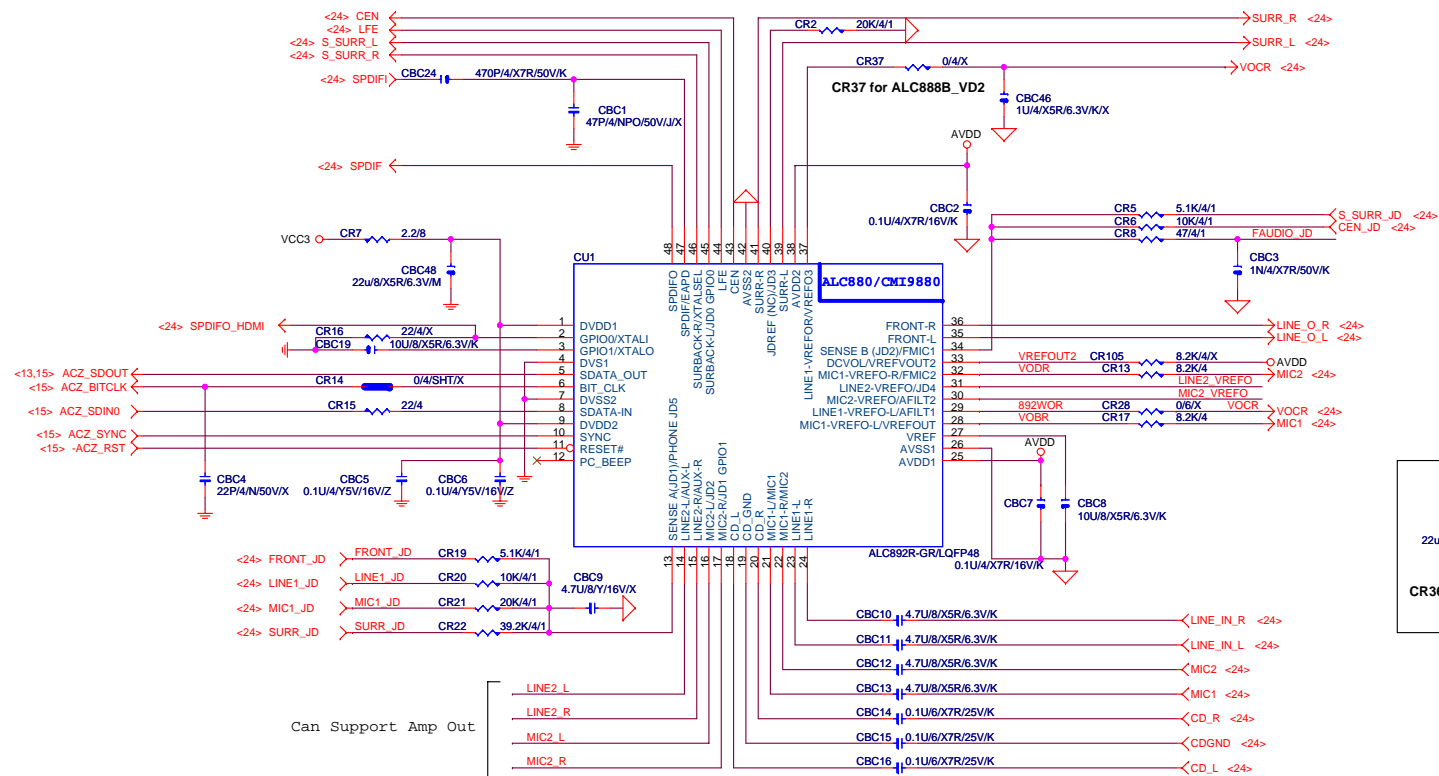


GIGABYTE

Title			FANHWMO
Size	Document Number	GA-M52LT-D3	
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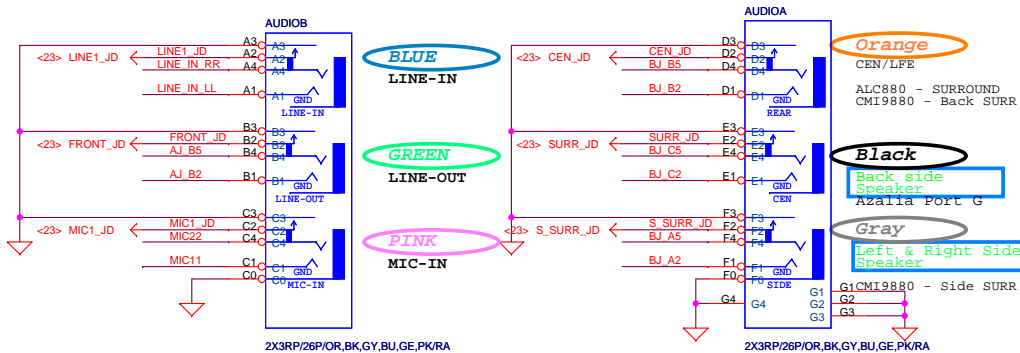
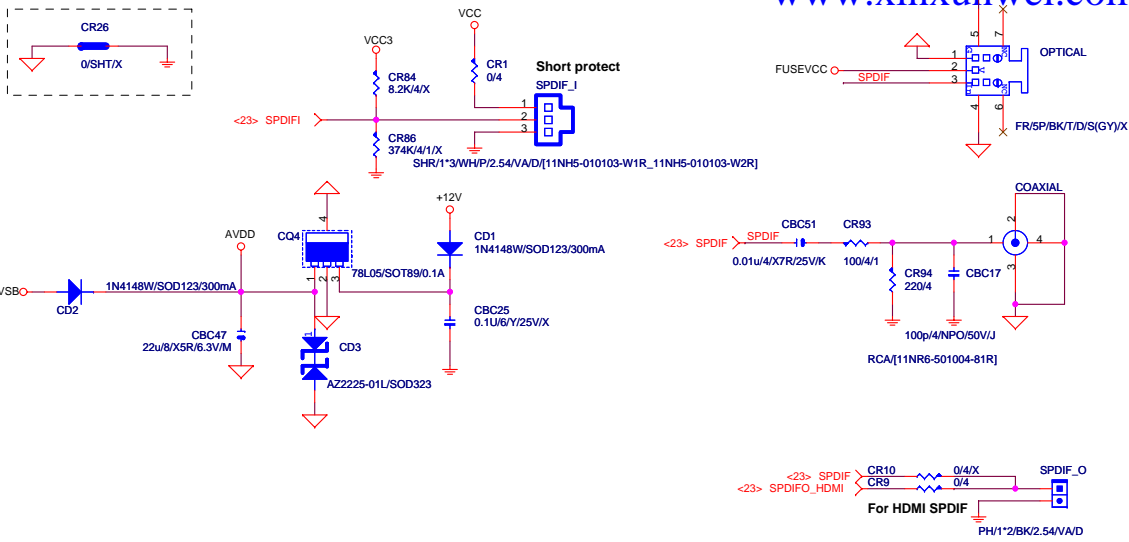






GIGABYTE

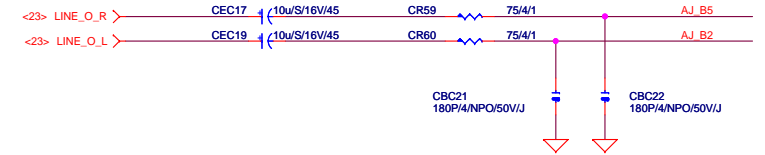
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Size	Document Number	GA-M52LT-D3	
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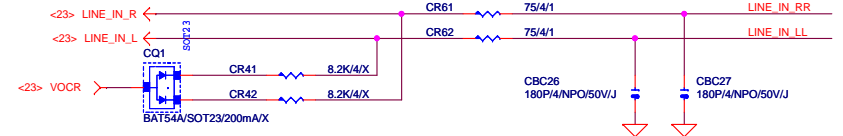
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3RJ+15F/[11NR6-403004-31]

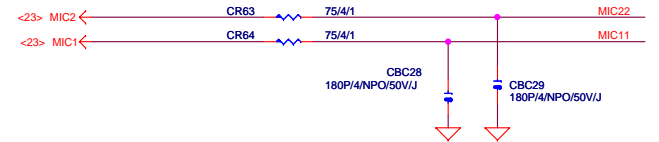
## LINE OUT FRONT OUT



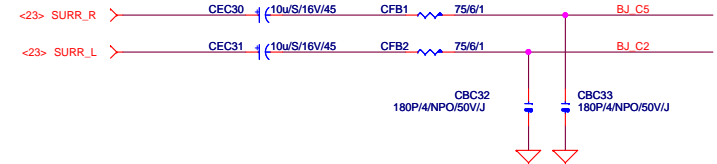
## LINE-IN



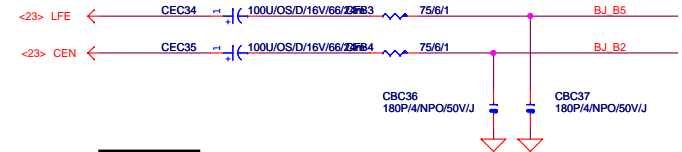
## MIC



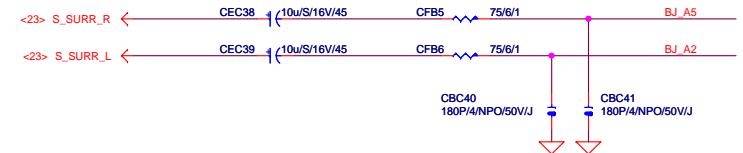
## SURROUND



## CEN/LFE



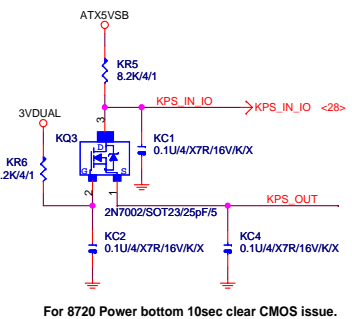
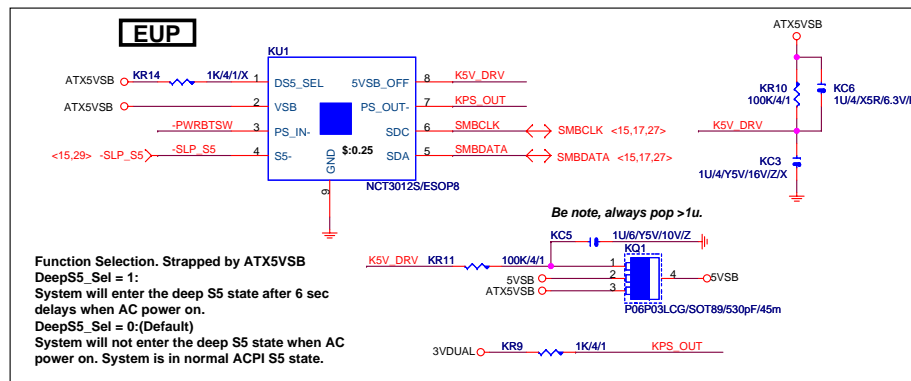
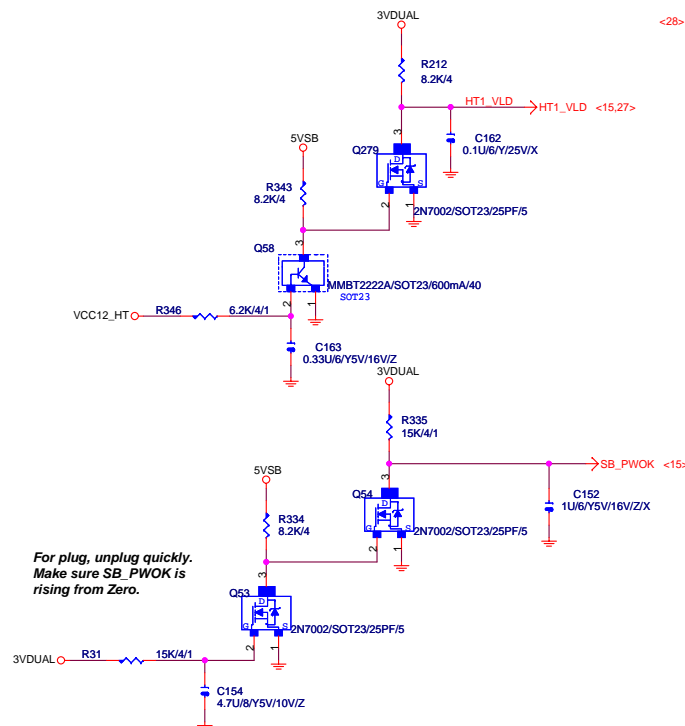
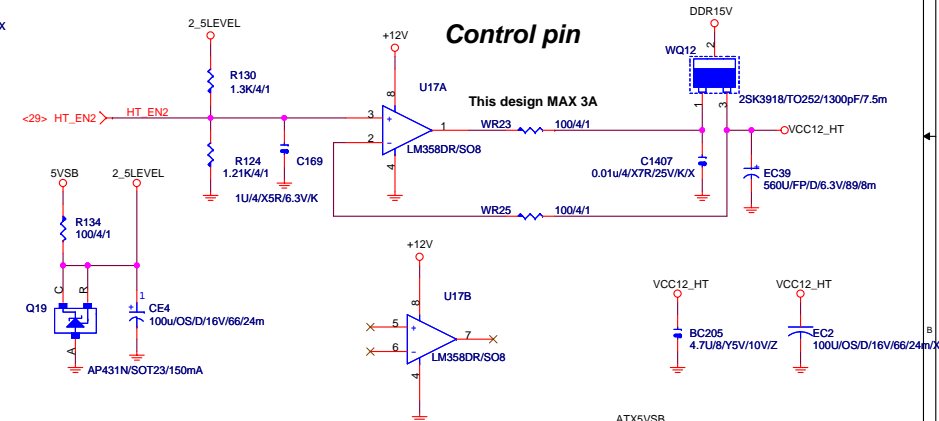
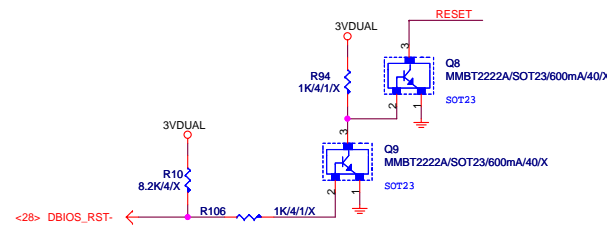
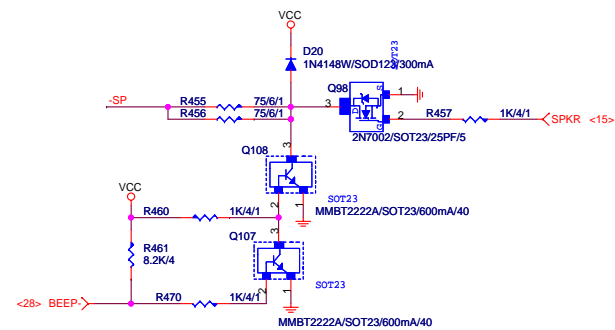
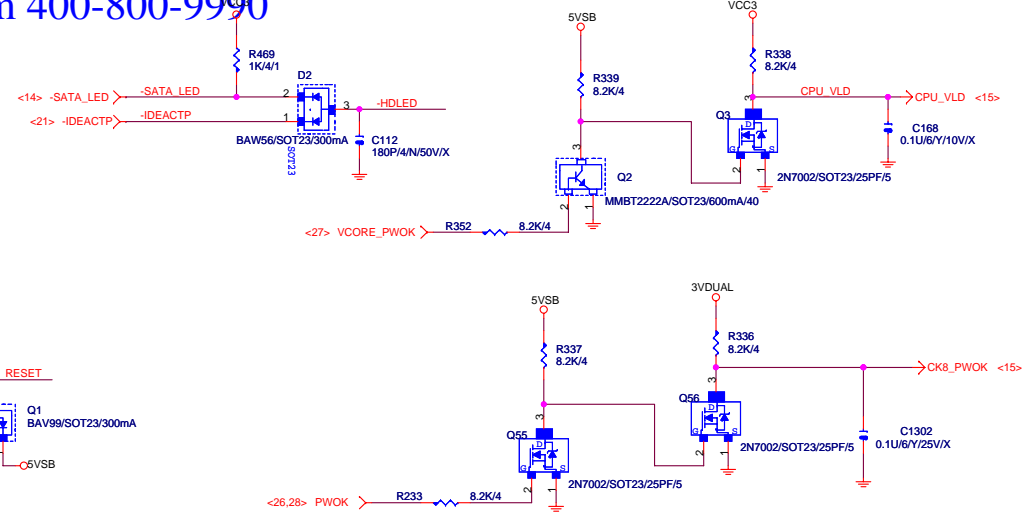
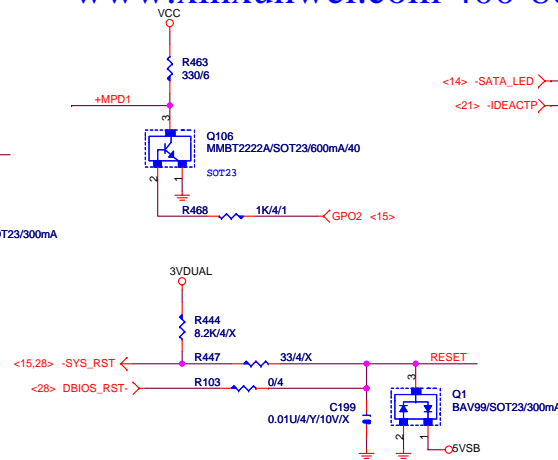
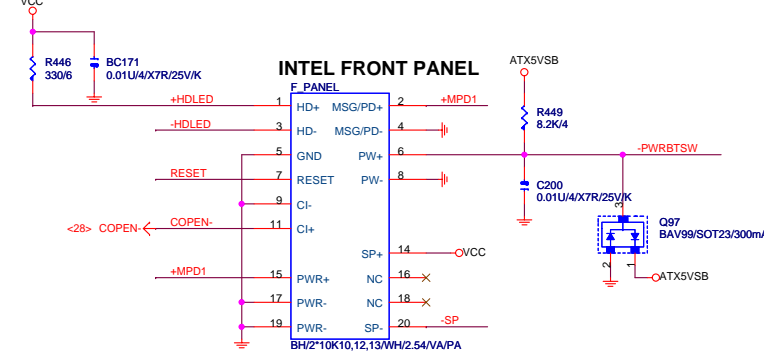
## SURR BACK



**GIGABYTE**

Title			
AUDIO JACK			
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**For plug, unplug quickly.  
Make sure SB\_PWOK is  
rising from Zero.**

**For 8720 Power bottom 10sec clear CMOS issue.**

<b>GIGABYTE</b>			
Title			
<b>FRONT PANEL</b>			
Size	Document Number		Rev
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## ATX POWER CONNECTOR

